ASTRONICS
TEST SYSTEMS

NO ESCAPE

Massively Parallel System-Level Testing – The New Paradigm for Semiconductor Quality Control

SOLUTION BRIEF

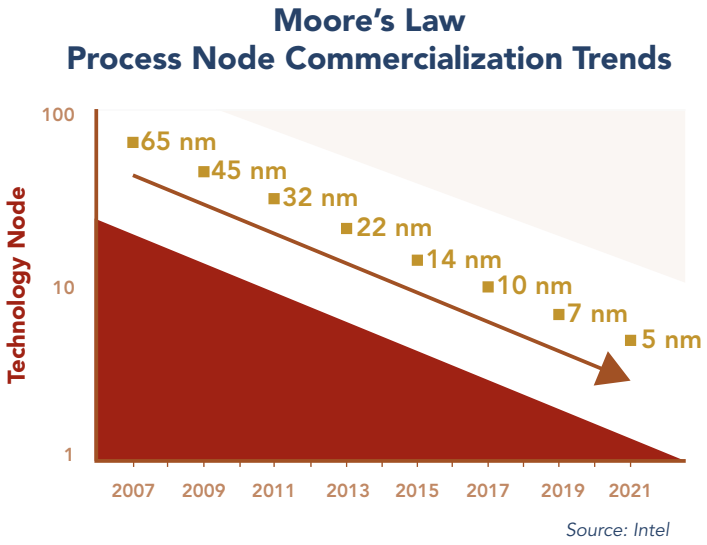
INTRODUCTION

Decades of advances in the semiconductor industry continue to drive an insatiable consumer demand for smaller, more powerful, more ubiquitous devices – whether in our cars, on our countertops or around our wrists. To meet this demand now and into the future, the fabrication of increasingly complex semiconductor systems for an incredible spectrum of applications must scale accordingly. Additionally, standards of quality control need to exceed current levels due to safety-critical applications and brand perception. Likewise, testing methodologies must evolve to address this emerging complexity and comprehensively evaluate devices under test (DUTs) for defects that appear in real-world conditions. Finally, they need to achieve the desired product yields with minimal impact in terms of time and cost. As the industry moves toward higher-volume fabrication of ever more intricate systems and zero-defect shipments, it has to create a new paradigm for quality control that also satisfies manufacturing needs. That paradigm is massively parallel system-level testing (SLT).

BACKGROUND

Smaller, Better, Faster, Moore

More than 50 years after Gordon Moore first posited the idea that the number of transistors per integrated circuit (IC) would double at a brisk and steady rate for the foreseeable future, we find ourselves close to mass fabrication of chips with feature sizes measured in nanometers and ICs that house billions of transistors. The pace and potential of this miniaturization are evident even to the layperson. All you have to do is compare the room-sized computers of the 1950s with the vastly more powerful one you have in your pocket today.

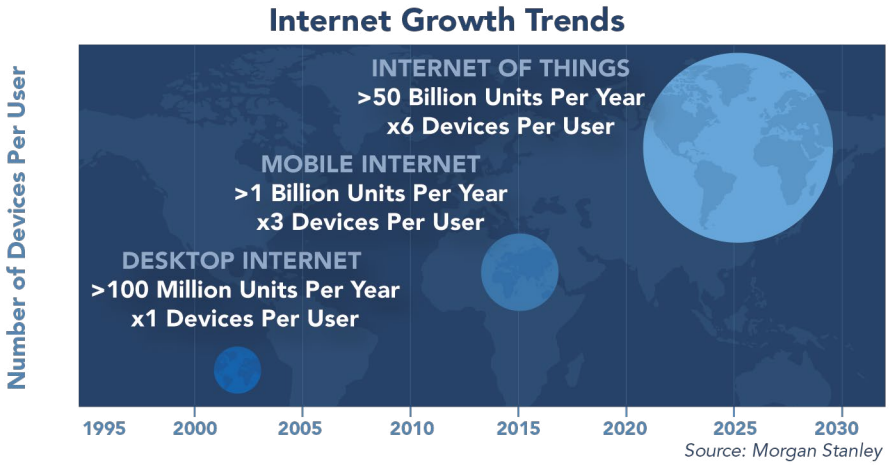


The familiar Moore's Law chart of the technology process node progression that enables the doubling of transistor count per IC, including the recent 3D transistor structures introduced at 14 nm.

It's not just our desktop and mobile computers that have become smaller and smarter. The mobile Internet era and its eventual successor, the Internet of Things (IoT), are introducing cloud-networked digital brains into everything from cars to tea kettles. This has been largely achieved by system-on-chip (SoC) technology, which packs the traditional hardware building blocks of processor, memory, storage, power management and even network communication into a single embedded system.

Yet it takes an incredible amount of intricacy, coordination and density to achieve this kind of elegant simplicity. In the automotive industry, for example, it's been found that a typical new car has roughly 30 microcontroller units (MCUs), with premium mid-range and luxury vehicles boasting more on the order of 100 MCUs – all to provide increasingly common features like tire-pressure monitoring, navigation and adaptive controls.[1] By 2018 semiconductor content alone is predicted to account for $610 per vehicle, making it a $32 billion market.[2] The International Technology Roadmap for Semiconductors (ITRS) 2.0 has already responded to these developments by stressing system integration, hyper-connectivity, the manufacture and integration of heterogeneous components, and the extension of Moore's Law into the third decade of the 21st century.

Looking at the waves of volume in terms of Internet growth drivers, where bubble sizes are proportional to total unit shipments.



Source: Morgan Stanley

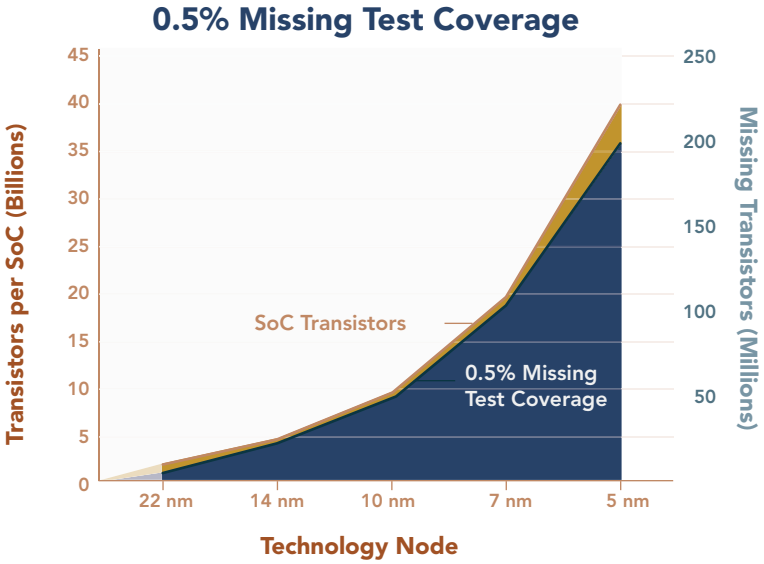
Testing, Testing, Testing

Although ITRS 2.0 and the many industries it affects are well aware of the challenges and opportunities that lie ahead, conventional semiconductor testing is at risk of falling behind emerging complex semiconductor manufacturing trends. As chips grow denser and novel 3D finFET stacking supplants classic 2D MOSFET structures, current-generation methodologies such as design-for-testability (DFT) and automated testing equipment (ATE) continue to catch the majority of defects early in the manufacturing process to prevent expensive escape costs downstream. But they don't catch them all.

With clock frequency and data transfer rate increasing within embedded systems, the limitations of these current-generation testing methodologies have started to show. For example, conventional ATE setups impose long traces between the DUT and the measurement tester resources, which introduces artificial propagation delays not present in real-world layouts. These real-world layout differences may seem insignificant; however, this subtle layout difference can enable the DUT to pass the ATE insertion yet fail in the destination application. Similar results are possible from subtle layout differences in power traces, grounding and heat-dissipation features. This means that conventional testing ends up missing critical defects and outliers that make their way into shipping products.

Just how much slips through the net? Taken together, ATE and DFT techniques offer typical 99.5% test coverage of DUTs in common implementations.[3] That might sound like an acceptable level of coverage, but scale has the potential to render it worryingly inadequate. With the number of IC transistors approaching tens of billions and semiconductor production volumes rising to meet the needs of, say, the $3.3 billion IoT industry (currently growing by approximately 23% annually) or the $9.4 billion wireless industry (approximately 20% annual growth), this leads to ever greater product shipments that have millions of untested transistors on each unit.[4] In addition to system complexity faults due to integration trends, this gap left by structural and functional test methodologies correlates to the increased likelihood of defective units escaping detection.

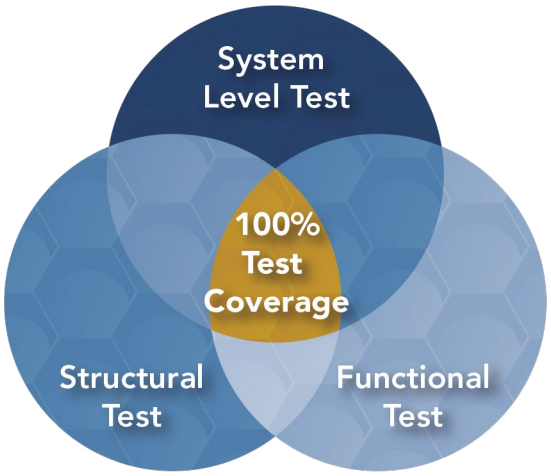
Proportional relationship shown between overall SoC transistor count (on left axis) and missing coverage (<1%) transistor count (on right axis).



SOLUTION: THE EVOLUTION IN TEST

No Escape: System-Level Testing

In the face of these shortcomings, system-level testing (SLT) is emerging as the essential new paradigm for significantly improving semiconductor quality and yields. SLT mimics real-world scenarios in terms of software, electronics and layout – such as testing the processor in the target application of an embedded system. For example, if a DUT is destined for use in a cloud-connected fitness tracker, SLT can virtually replicate the actual conditions under which that embedded system will function. By closing the gap between mere component testing of DUTs and actual performance as experienced by the consumer, SLT ensures the 100% test coverage that is vital in preventing defect escapes.

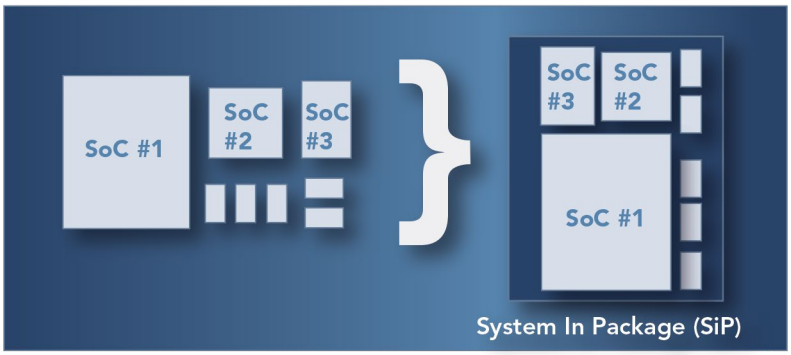


The mesh of structural, functional and system level test ensures 100% test coverage.

However, for many semiconductor and device manufacturers, time, costs and other resources have been traditional barriers to implementing more holistic testing methodologies that include SLT. With each additional testing stage, or insertion, the cost of test (CoT) increases, which is usually proportional to the time required for testing. Typically this amounts to only a few cents and seconds per unit – yet, once again, these aggregate numbers are significant when one considers the scale of manufacturing. Pennies and seconds add up.

Time to volume (TTV) and cost are also factors driving a transition to advanced system packaging, which in turn is driving a transition to SLT. One such example is the recent packaging innovation of system-in-package (SiP) over individual SoCs on account of their shorter design cycles and reduced bill of materials. SiPs also bring advantages when it comes to miniaturization, power draw, performance, and — in line with ITRS 2.0 — the integration of heterogeneous systems. This makes them ideal for application in markets like wearable devices, which are predicted to soar to 295 million units per year by 2020 across the consumer, healthcare and industrial markets.[5] At the same time, the intrinsic complexity of SiPs calls for comprehensive quality-testing methodologies like SLT that are able to evaluate more than just the structural or functionality integrity of block-level parts.

Industry is accelerating device complexity through innovative packaging technology (e.g., SiP) that involves integrating multiple known-good-die (i.e., SoC) into a single packaged device.



The True Cost of Testing

Despite its obvious advantages, many companies weigh the additional cost of SLT and wonder whether they can afford it. The truth is, they can't afford not to.

When a defective unit escapes into consumer hands, there are return material authorization (RMA) costs, supplier penalty fines and even potential lawsuits, not to mention lasting brand damage that can jeopardize customer loyalty and public perception. In some applications, lives are at stake. This is why, even as DUTs become denser and more complex, the automotive, biomedical and aerospace industries in particular, along with their regulatory bodies, will not tolerate test methodologies that aspire to anything less than zero defects. For instance, in the automotive sector, we are currently witnessing a shift in quality tolerance from 50 defective parts per million (dppm) to a level of less than 10 defective parts per billion (dppb) – zero defects for all intents and purposes. Cutting corners for the sake of CoT could very well send customers and distributors looking for someone who won't.

Existing test methodologies can also err in the opposite direction by flagging sound DUTs as defective. This results in overkill, with perfectly good units consigned to the scrap heap. SLT helps avoid these false positives and increase yield. This, along with the many other reasons given above, is why many manufacturers of mission-critical components will likely migrate to 100% SLT as a best practice in their production flow.

MAKING SLT AN AFFORDABLE REALITY

Performing SLT at an affordable cost has been challenging. Solutions to date require manufacturers to buy many testers in a typical x6 configuration with less than 100 UPH to handle the load. This scaling effect leads to the cumulative need for not just more testers, but for more operators, more factory floor footprint, and more cost. To make 100% SLT an effective strategy, innovation in replacing many lower-UPH testers with a single higher-UPH tester is desirable.

One idea is to implement SLT testing in massive parallel, with up to hundreds of DUTs tested simultaneously. Astronics Test Systems has helped a few of the world's largest semiconductor companies adopt this approach over the last several years, with excellent results. However until now solutions have been provided to these organizations on a custom-designed basis.

Now Astronics Test Systems is introducing a standard semiconductor test solution that renders high volume, 100% SLT affordable. This next-generation methodology mitigates the challenges of SLT by offering an automated massively parallel architecture to achieve a high overall unit per hour (UPH) production to keep escalating CoT in check.

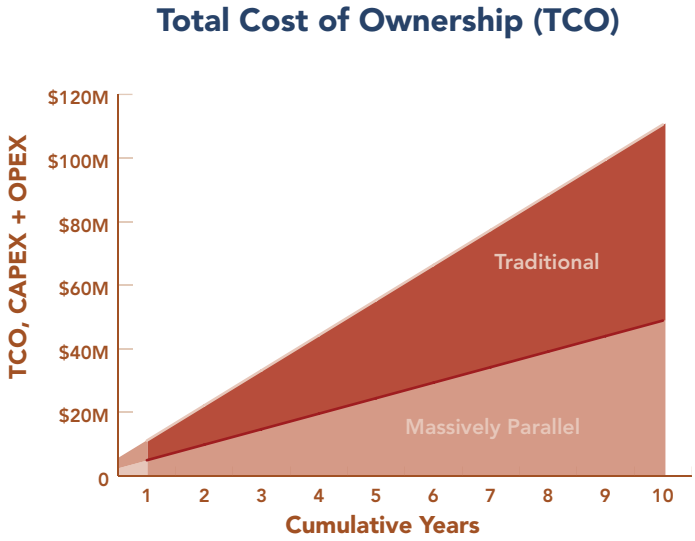
The new ATS 5034 System-Level Test Platform is the culmination of more than 20 years of experience in high-volume burn-in and SLT with a track record of more than 9 billion processors tested over three generations of field-proven testers. It incorporates layout emulation, boot sequence and application testing directly into the SLT insertion to maximize efficacy while minimizing production impact. Despite its small factory footprint, the innovative ATS 5034 SLT Platform leverages a massively parallel architecture to test integrated semiconductors in this far more holistic "mission" mode at industry rates of up to 5,000 UPH.

The ATS 5034 SLT Platform reduces CoT by delivering massive parallelism and up to 5,000 UPH.

Along with high-volume capacity, the implementation process is optimized with CoT and TTV in mind. An engineer can design a test sequence for a single site, and the ATS 5034 SLT Platform easily and automatically scales that sequence to hundreds of sites through its proven ActivATE™ test executive software. As a turnkey solution, designed by test engineers for test engineers, the ATS 5034 SLT Platform empowers manufacturers to augment existing testing methodologies with a seamless and rapid transition to 100% SLT. The benefits are quick and easy to achieve.

Furthermore, the ATS 5034 SLT Platform serves the demands of ITRS 2.0 as well as forthcoming trends and advances. It tests a wide range of semiconductor devices, such as microprocessors, microcontrollers and embedded systems—including support for SoCs, modules and heterogeneous SiPs—with an extremely accurate thermal stress testing capability of +/– 1°C (typical).

Compared to competing SLT solutions, this new slot-based asynchronous massively parallel platform offers significant technological advancement plus distinct bottom-line advantages in terms of footprint, UPH, scalability, increased yield, operation and testing. The collaborative engineer-to-engineer environment at Astronics ensures that this system can be tailored to suit a customers' exact needs. Experienced global installation, maintenance, and support teams satisfy even the most aggressive product ramps.



Analyzing the cumulative cost for five (or ten) years reveals the 2:1 cost savings potential compared to popular competitive offerings (x6 sites)

CONCLUSION

SLT enables manufacturers to balance the conflicting demands for more complete defect screening of increasingly complex devices and a push for zero-defect shipments across multiple industries. As a result, 100% SLT is rapidly emerging as a best practice throughout the semiconductor ecosystem as a complementary testing methodology to structural and functional tests. Through massive parallelism and industry-leading high-throughput UPH, the new ATS 5034 SLT Platform from Astronics Test Systems provides an easy path for manufacturers to transition to SLT while achieving CoT and TTV goals.

Sources:
1. McKinsey & Company, *Winning Share in Automotive Semiconductors*, 2013
2. IC Insights, *IC Market Drivers Report*, 2014
3. SemiEngineering.com, *Balancing the Cost of Test*, 2014
4. IC Insights, *Cell Phones Continue to be the Largest Driver of IC Sales*, 2014
5. Yole, *Consumer, Healthcare, and Indutrial Will Drive the Rapidly-Expanding Wearable Industry to a Potential Value of $90B by 2020*, 2015

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